accessing a virtual address in said associated TLB; locating an associated physical address corresponding to said virtual address;

sending a TLB message from one of said plurality of processors to said main communication network if (1) a first entry was input when said corresponding associated physical address was not located; (2) a second entry within said corresponding associated physical address was moved to another location within said computer system; or (3) said second entry was removed; and

sending said TLB message from said main communication network to said plurality of processors.

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8. (Once Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for maintaining TLB coherency in a computer system having a plurality of processors, each of said processors having an associated TLB for storing an address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in said associated TLB; locating an associated physical address corresponding to said virtual address;

sending a TLB message from one of said plurality of processors to said main communication network if (1) a first entry was input when said corresponding associated physical address was not located; (2) a second entry within said corresponding associated physical address was moved to another location within said computer system; or (3) said second entry was removed; and

sending said TLB message from said main communication network to said plurality of processors.

9. (Once Amended) An electronic data processing apparatus, comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors distributed among said said plurality of independent paths with each said processor connecting to one of said plurality of independent paths; and

a TLB message generator for accessing a data address and transmitting a TLB message on said plurality of independent paths.

12. (Once Amended) A system for TLB coherency in a computer system, comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors distributed among said plurality of independent paths with each processor and its associated TLB connecting to one of said plurality of independent paths;

means for performing an access to a data address from its said associated TLB;

a TLB message generator for generating TLB message; and

means for transmitting said TLB message and said access data to a main communication network.

13. (Once Amended) The system of claim 12, further comprising means for transmitting said TLB message and said access data on said plurality of independent paths and comparing said accessed data address with an address translation data of the information stored in each of

said plurality of TLBs, said TLB message informing each of said plurality of TLB if said access data address affects data stored therein.

14. (Once Amended) The system of claim 12, further comprising means for adding said access data address into said associated TLB in each of said plurality of processors.

15. (Once Amended) The system of claim 12, further comprising means for invalidating said address translation data in said associated TLB in each of said plurality of processors.

16. (Once Amended) The system of claim 12, further comprising moving said address translation data in said associated TLB in each of said plurality of processors to another part of the computer system.

17. (Once Amended) The system of claim 12, wherein the TLB message further comprises:

a read access message if said accessed data address is inputted into said associated TLB.

18. (Once Amended) The system of claim 12, wherein the TLB message further comprises:

a write access message if said accessed data invalidates said address translation data in said associated TLB.